

FIG. 1

200

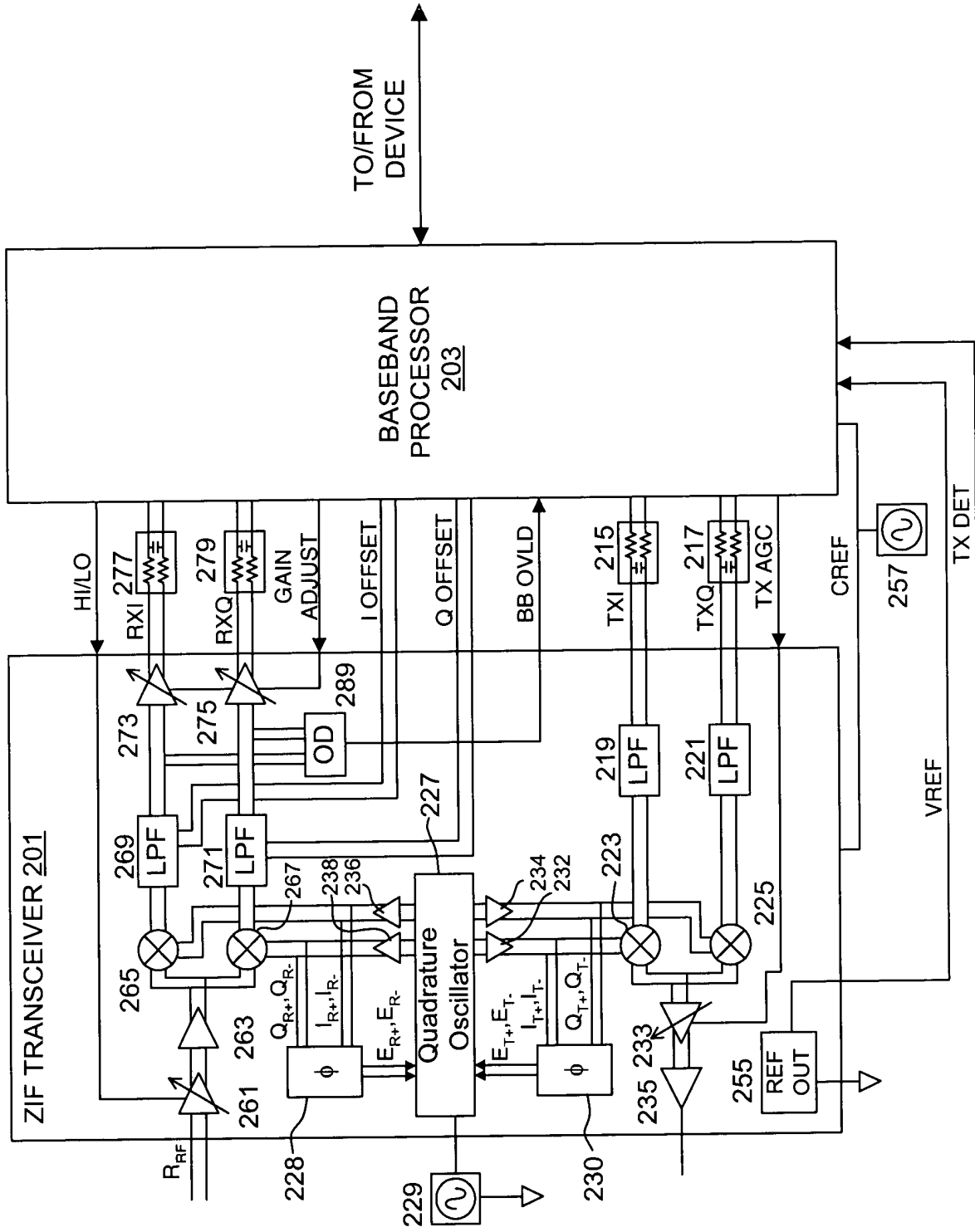


FIG. 2

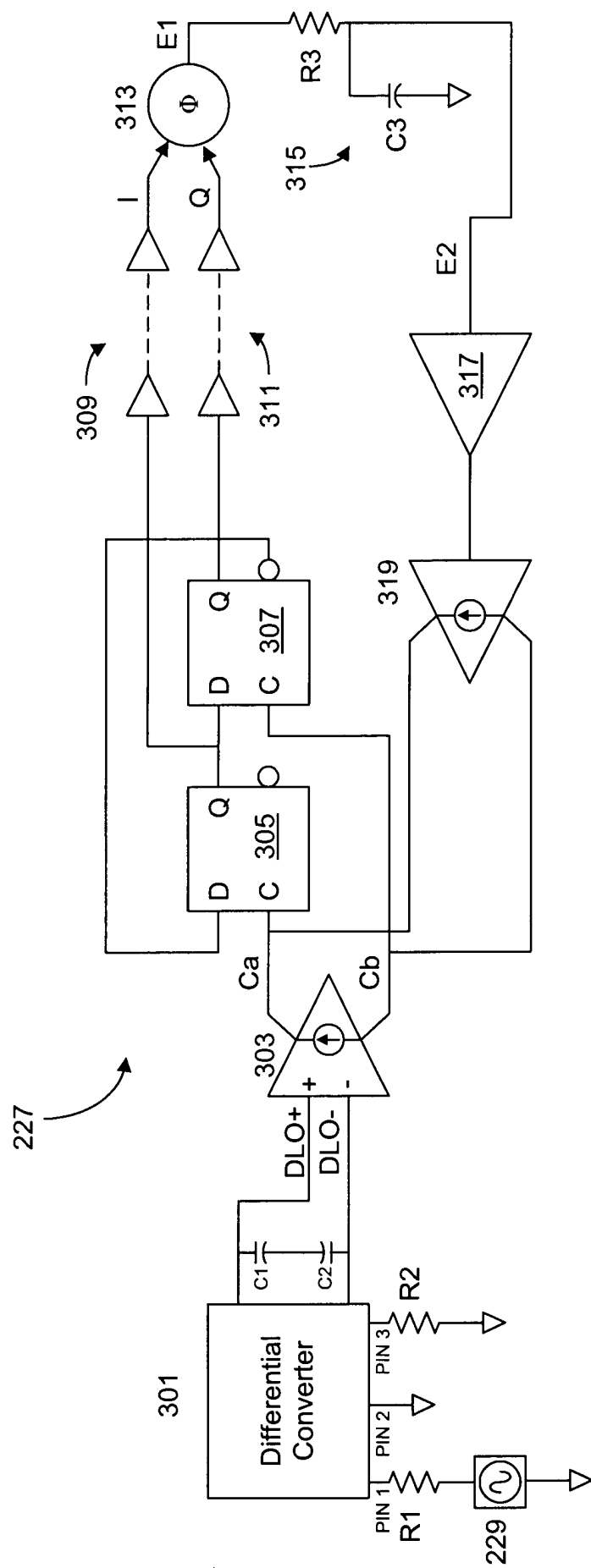


Fig. 3

FIG. 4 is a schematic diagram of a circuit for generating a differential output signal. The circuit includes a differential pair of transistors Q1 and Q2, a differential pair of diodes Q3 and Q4, and a differential pair of capacitors C1 and C2. The circuit is connected to a differential output signal DLO+ and DLO-.

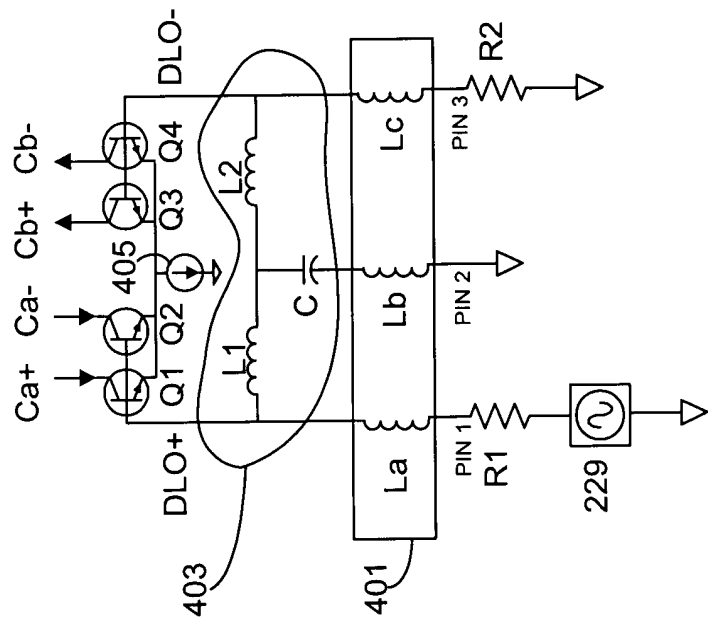


FIG. 4

500

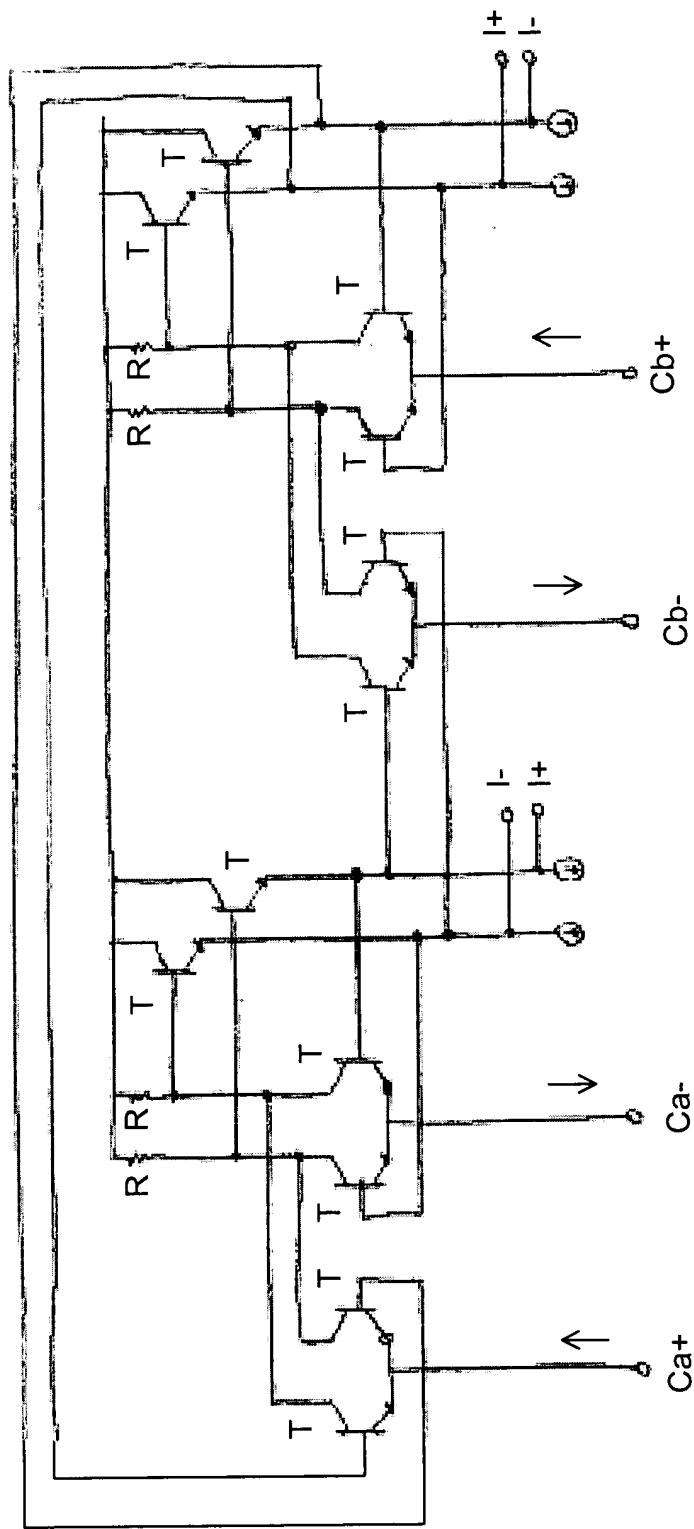


FIG. 5

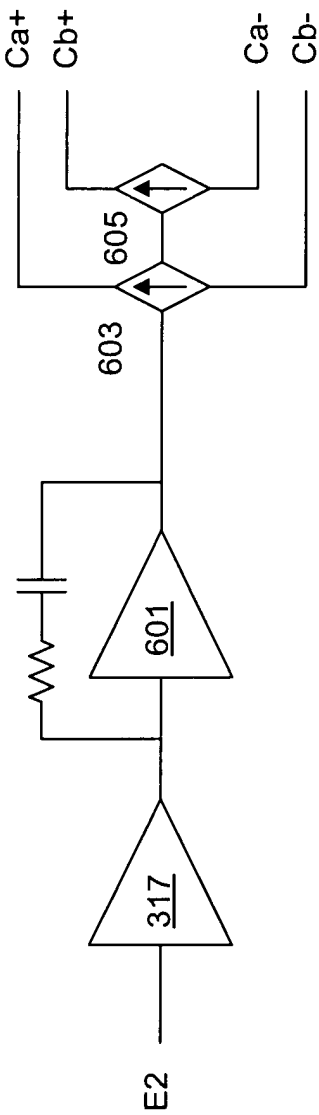


FIG. 6

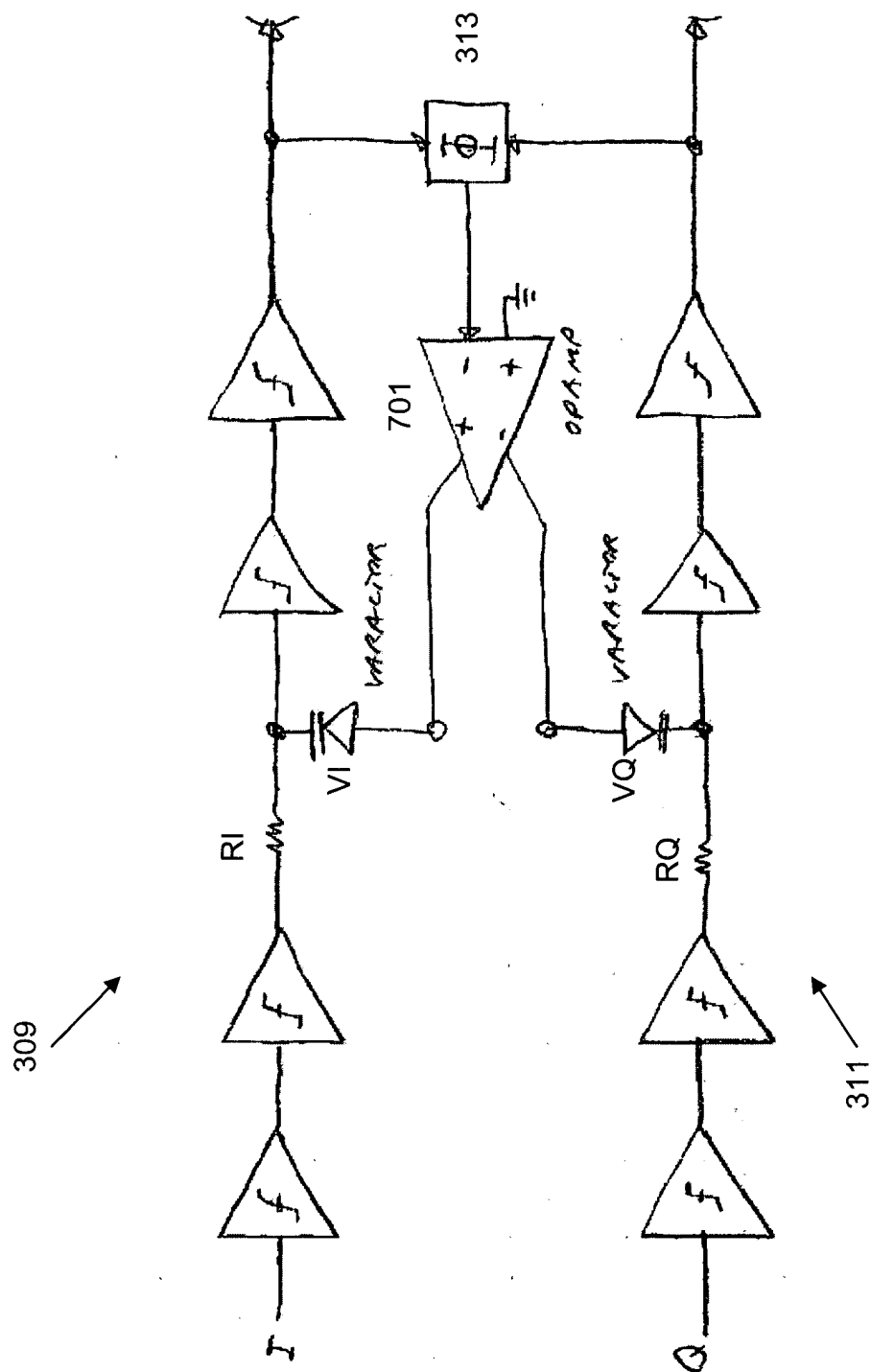
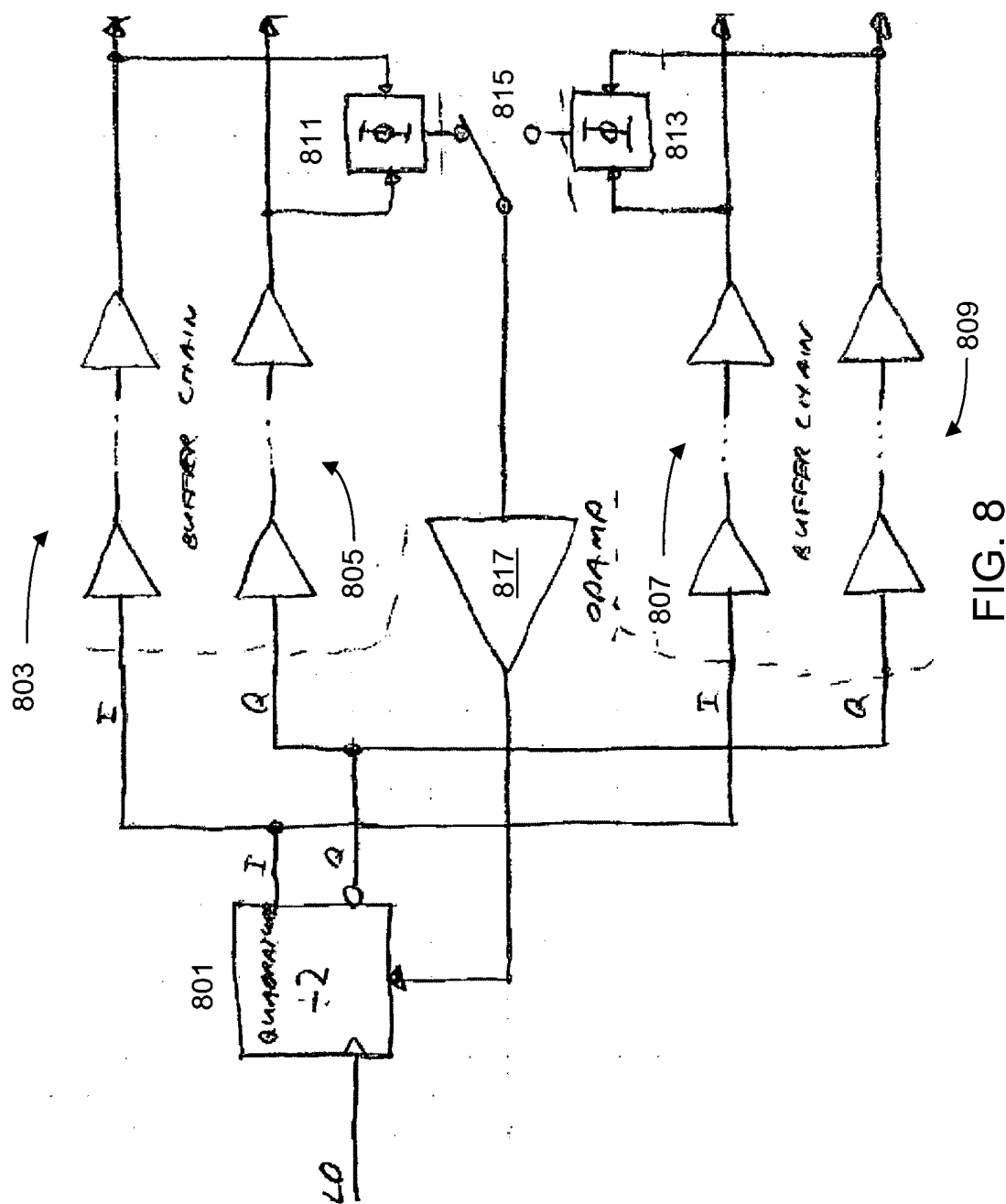


FIG. 7





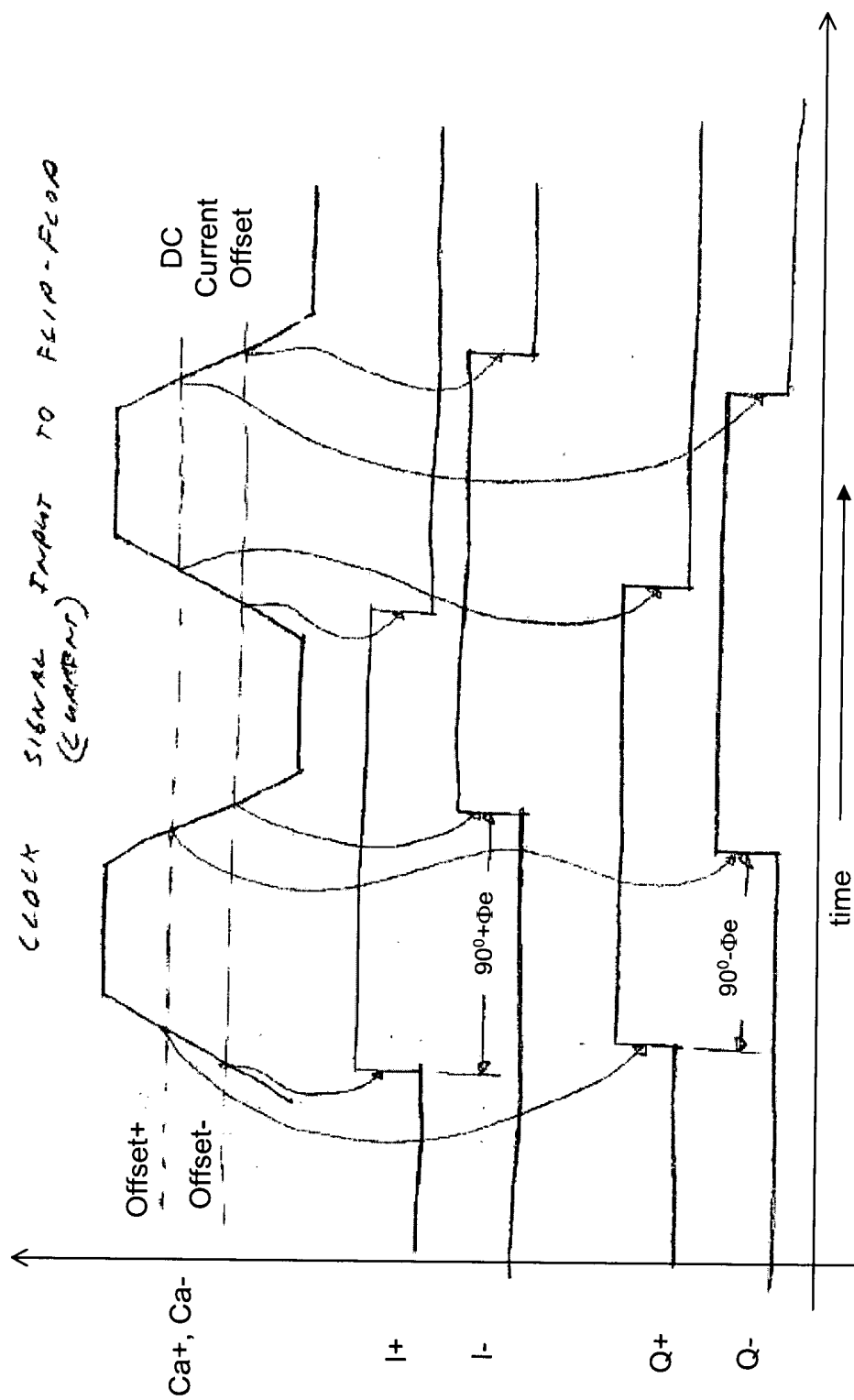


FIG. 9